Ashwini K. Nanda, Ph.D.

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Los Angeles, CA 90019, USA

Internationally recognized expert, thought leader and researcher in high performance computer architecture and supercomputing systems, and Applied AI. Pioneered hybrid HPC technologies including world's first Petaflop supercomputer and other Top500 supercomputers in the US, EU and India. Numerous high impact patents, publications and products; an IEEE Fellow, and Fellow of Asia Pacific AI Association.

EXPERIENCE HIGHLIGHTS

Honorary Chair Professor, TIH, IIT Guwahati, Adjunct Prof, IIT ISM Dhanbad, *May 2026 ---*
Initiated the formation of a Biomedical Engineering and Science Research Center (including an academic program) at IIT ISM Dhanbad. Initiated several Applied AI projects at TIH, IIT Guwahati.

Founding Center-Director, AHRC and Visiting Professor, Computer Science *Mar 2023 --- Mar 2026*
Adjunct Professor, Computer Science, 2008-2023
Founding Center Director, AI and HPC Research Center (AHRC), and Visiting Professor, Computer Science and Engineering, Indian Institute of Technology, Bhubaneswar, India.

• Established an Institute Research Center, AI and HPC Research Center (AHRC) at IIT in Dec 2023. Designed as an interdisciplinary National Research Center based on the novel idea of an open collaboration platform. Built a national and global alliance of 100+ professionals in multiple disciplines in 30+ national and global institutions involved in Applied AI in academia/industry and govt.
• Major funding as PI: 1. Rabisons Foundations Endowment Grant for Research in Applied AI, Rs 25 CR, 2. NSF-MeitY US-India joint project on Eco-LLM: Energy Efficient Computing and Communication Architecture for LLMs, Rs 11 Cr, SPARC: 70 Lacs, ANRF: 1.5 Cr
• Major partner in consortium led by IIT Ropar, MoE CoE in AI/Agriculture, Rs 330 Cr Total for consortium, and in consortium led by IIT Delhi/AIIMS Delhi, MoE CoE in AI/Medicine, Rs 330 Cr for consortium
• Released 10 SW/HW products, TRL level 4-7 in AI/Medicine, AI/Transportation and AI/Agriculture, Submitted 5 patents to IIT patent office, 6 research papers accepted/published in journals/conferences, 10 papers under submission/review
• Established a new PhD program in Applied AI at AHRC, IIT Bhubaneswar. Led the development of the MTech in AI program for the CSE dept. Trained 60+ PhD/MTech/BTech students and 100+ interns in Applied AI skills, brought awareness on importance of Applied AI in job creation to 1000+ students/faculty/researchers around the country by conducting workshops, seminars and lecture.
• Taught courses in computer architecture, high performance computer architecture, Applied AI, Machine Learning, Advanced topics in AI and Architecture

Founder and CEO *Jan 2009 ---*
HPC Research Inc., USA, HPC Links, India, www.hpclinks.com

• Recently architected and provided software solution for securing 5000 servers of RBI from hacking and cyber threats at National Payments Corporation of India (NPCI). Architected and provided hardware/software cyber security systems for protecting critical electronic infrastructure in the factories of Reliance Industries.
• Data analytics and cyber security projects for ONGC, Indian Army, Reliance Industries, NPCI.
• Significant business impact to Fortune500 companies thru parallel application scaling and cluster software services, including Microsoft, GE, NVIDIA, NEC Research, Reliance Industries, ONGC and Govt. of India.

• Introduced two new HPC sw products in the market. (1) VERTEX: a cluster software platform product for heterogeneous HPC clusters. Used by US Air Force, Total Research, Supermicro and AWE (UK) among others.
• (2) QuantApps: A quantitative finance based tool for algorithmic trading targeted for small and medium investment firms. Five Indian customers reaped over 50% of annual profits on investments using QF Links.

Head/CEO of Tata CRL, HPC Business/market strategy head, Tata Group *June 2007 to Jan 2009*
Computational Research Laboratories (CRL), Tata Group, Pune, India

- As the Head of CRL, led the development of Eka, Asia's fastest supercomputer (2007). Helped create the weather/atmospheric modeling platform for India's maiden lunar mission Chandrayaan, several scalable applications including genome sequencing, fluid dynamics, and seismic modeling.
- Developed HPC technology, business and market strategy for Tata group that laid the foundation for a follow-on high end HPC services business worth over $200M.

Chief Architect and Dept. Manager, Cell/Quasar Systems *2005 to May 2007*
IBM Systems and Technology Group, NY - Co-led the establishment and operation of 400+ members strong, globally distributed Quasar/Cell Systems Design Center. Led hardware, software, and systems roadmap, architecture and product plan definition for an estimated $1B+ business over next 5 years.

- Three generations of blade products, QS20, QS21 and QS22 launched successfully. Major HPC system deals including LANL Roadrunner (World's 1st PetaFLOP system) and Sony Cell World Server signed.
- These and other deals resulted in ~$250M in sales and/or committed revenue for Cell-based systems.
- Shaped IBM's strategic systems partnerships with major corporations around the globe, including Sony, Toshiba, Mercury Computers, Mayo Clinic, Pixar, Chase, DoD and Los Alamos National Labs (LANL)

Chief Scientist and Research Lead, Cell-Based systems *2003 to 2005*
IBM TJ Watson Research Center, Yorktown Heights, NY - Pioneered the concept of heterogeneous clusters.
- Architected, developed and built first generation Cell blade prototypes for customer engagements and software development. Led development of several application prototypes, software tools and compilers. Grew the IBM-wide virtual team from virtually zero to over 200+ members to work on Cell systems.
- Convinced IBM senior executives, business and technical leaders about the technical viability and significant system business potential of the revolutionary, low power/ low cost Cell processor platform.
- Provided technical leadership for signing of a major deal with Mercury Computers. Critical role in signing and executing major contract with the US government. These contracts led to over $150M revenue.
- Started research relationships with 20+ partners including Stanford, Illinois, UPC, USC, LANL and LLNL.

Manager, Research Staff Member, Tech. Staff to VP Research *1995 to 2002*
IBM T.J. Watson Research Center, Yorktown Heights, NY

- Technical Assistant to the VP of Systems in 2002. Led research strategy and helped manage operations for the ~500 member strong organization. Led the Systems part of the Global Technology Outlook for IBM.
- As Research Staff member and Manager, 1995-2001, established and led a twelve-member research team and the scalable shared memory systems research program, critical to the products from IBM NUMAQ division. Developed a Real Time hardware analysis tool (MemorIES) that helped improve memory system design in IBM server products, and was adopted by MIT, U. Mich., and USC as a research platform.

Other Experience *1983 to 1995*

- 1993-1995: Texas Instruments, Dallas - Co-architected an Intel x86 compatible processor. Invented new processor design concepts such as atomic operations and misprediction recovery cache.
- 1986-1988: Senior Engineer, Wipro Information Technology Ltd, Bangalore, India: Led development of parallel processor systems for India's Missile Defense program and system hardware development
- 1983-1984: Computer Hardware Engineer at the Computer Science Center, Tata Motors, Jamshedpur, India

EDUCATION AND TRAINING

Ph.D.: Computer Science, Texas A&M University, College Station, Texas (GPA 4.0/4.0). 1989-1993
Dissertation Title: "Design and Application of Cache Coherent Multiprocessor Systems"
M. Tech.: Electrical Engineering, Indian Institute of Technology, Madras (High Honors) 1984-1985
B.Sc. (Engg.): Electronics & Comm. Engg, Sambalpur University, India, (Ranked #1 in University) 1978-1983
(Distinguished Alumnus award at Diamond Jubilee in March 2017)

- MIT Sloan School of Management: Entrepreneurship Development Program, 2006
- Wharton Business School: Executive Leadership program, 2007, Executive Competencies training at IBM

MAJOR FUNDING SUCCESSES

IBM Cell Server pilot - $3M, IBM Cache memory emulation - $3M, LANL Roadrunner supercomputer - $120M (IBM TJ Watson + Server group), NEC Research - $600K, Tata Eka system - $8M, AHRC Rabisons endowment – Rs 25Cr, NSF-Meity – Rs. 11 Cr, other projects from DoE, ANRF, DST etc. between 1-3 Crs.

PATENTS

Thirteen(13) granted US patents in the area of computer architecture, systems and parallel processing.

Impact: All the patents have either been implemented in real processor and system designs, or used for further research in both academia and Industry. The patent on misprediction recovery cache invented a completely new mechanism, used by the Texas Instruments Amazon processor, and was named the most influential patent by 'Microprocessor Report'. The paper on this idea was awarded the best paper in the ACM/IEEE Micro conference. The patents on directory caches, protocol engines, CCR, coherence directories etc. were implemented in the IBM NUMA-Q shared memory server system. Many of them in some modified version are used widely in today's CPU products and servers from Intel, IBM, HP and others. These ideas also influenced further research in leading labs such as Stanford, Univ of Illinois, Univ of Wisconsin, Intel, IBM and HP. The patent on cache emulation was used to advance the state of the art in server design research at MIT, Univ of Michigan, Univ of Southern California and other leading universities. IBM used this patent to optimize L3 cache designs and operating system performance in bus based SMP systems.

	US Patent#	Title
1	8,838,674	Plug-in accelerator
2	7,925,485	System and apparatus for managing latency-sensitive interaction in virtual environments
3	7,624,222	South bridge system and method
4	6,965,972	Real time emulation of coherence directories using global sparse directories
5	6,826,651	State-based allocation and replacement for improved hit ratio in directory caches
6	6,792,512	Method and system for organizing coherence directories in shared memory systems
7	6,721,858	Parallel implementation of protocol engines based on memory partitioning
8	6,628,615	Two level virtual channels
9	6,405,292	Split pending buffer with concurrent access of requests and responses to fully associative and indexed components
10	6,338,123	Complete and concise remote (CCR) directory

11 6,038,645 Microprocessor circuits, systems, and methods using a combined writeback queue and victim cache

12 6,032,225 Microprocessor system with burstable, non-cacheable memory access support

13 5,881,277 Pipelined microprocessor with branch misprediction cache circuits, systems and methods

** Submitted 5 Indian patent applications to IIT patent office for filing in Jan/Feb 2026

SELECTED PUBLICATIONS

New publications at IIT BBSR:

1. Ashwini K Nanda, Madhusmita Sethy, Prajna Paramita Giri, Om Saran, K S Nataraj, Ajit Sahu, Satish K Panda "AI-Enhanced Cervical Cancer Screening for Improved Diagnosis" ESMO 2025, Berlin, Presented on October 17-21, 2025
2. Ashwini K Nanda, Sourav Mishra, K S Nataraj, Deepthi Sai, Mathukuri Likhitha "Predicting Chemotherapy-Related severe Haematological Toxicities in Cancer Patients using Machine Learning" ESMO 2025, Berlin, Presented on October 17-21, 2025
3. V K Ravidas , J Saravanan , Ashwini K Nanda, "AR-Based Visual Navigation & Safety System for Open-Cast Mines", to be presented at ICCMS 2025, IIT Bhubaneswar, Dec 17-19
4. Satish K Panda; Rituparna Addy; Ashwini K Nanda; Rajiv Raman. Artificial Intelligence for Monitoring Anatomical Response to Anti-VEGF Therapy in Macular Edema, ARVO 2026 (Investigative Ophthalmology & Visual Science), Denver
5. Satish K Panda, Tishya Chattopadhyay, Ashwini K Nanda, Rishikesh Rajendra Balvalli, SmartEye: An AI-Driven Mobile System for Automated Cataract and Pseudophakia Detection, WOC, World Opthalmology Congress, 2026, Prague
6. Tey, Kai Yuan, Brian Juin Hsein Lee, Clarissa Ng, Qiu Ying Wong, Satish K. Panda, Amrit Dash, Jipson Wong, Ashwini K Nanda et al. "Deep learning analysis of widefield cornea endothelial imaging in Fuchs dystrophy." Ophthalmology Science (2025): 100914.

Submitted Papers at IIT BBSR

7. Atnurkar, A., Ashwini. K Nanda, Panda, Sudhanshu S., Amatya, D., et al. 2025. *Advancing Forest Evapotranspiration Modeling: Machine Learning-Based ET Prediction using ECOSTRESS and SMAP Data*. Submitted to Remote Sensing (MDPI)
8. Panda, Sudhanshu. S., Atnurkar, A., Nanda, Ashwini K., Amatya, D., et al. 2025. AI Based Forest Evapotranspiration-Soil Moisture-Biomass Correlation Analysis in Southeastern United States with ECOSTRESS, SMAP, and GEDI Based Remotely Sensed Information. Submitted to the Journal of ASABE.
9. Rajesh Thiriveedhi, K S Nataraj, Sudhanshu Sekhar Panda, and Ashwini K Nanda "US Cotton Price Forecasting Using Linear Forecasting Machine Learning Models and Exogenous Variables" Submitted to Computers and Electronics in Agriculture.

10. Shakti P. Rath, K. S. Nataraj and Ashwini K. Nanda, "Self-Supervised Learning using Next Step Prediction and Maximum Entropy Losses for ASR for Low Resource Languages", Submitted to IEEE Transactions On AUDIO, SPEECH AND LANGUAGE PROCESSING, Dec 2025.

11. Chakraborty, and Subhransu Ranjan Samantaray, Ashwini K Nanda, "A New Charging Strategy to Reduce Long Queue in EV Charging Station with Grid Integration" (Communicated in IEEE Transaction on Power Delivery)

Earlier Publications

Books and Chapters

- D. R. Kaeli, H. Hadimioglu, J. Kuskin, A. K. Nanda and J. Torrellas, "High Performance Memory Systems," Springer-Verlag, 2004.
- A.K. Nanda and L.N. Bhuyan, "Design and Analysis of Cache Coherent Multistage Interconnection Networks," Interconnection Networks for High Performance Parallel Computers, ed. I.D. Scherson and A.S. Youssef, IEEE Computer Society Press, 1994.

Refereed International Journals

- P. Hofstee and A.K. Nanda, "Guest Editor's Introduction", IBM Journal of R&D Special Issue on Cell Broadband Technology and Systems, Sept. 2007.
- A.K. Nanda, J. R. Moulic, R.E. Hanson et. al., "Cell Blades: Building Blocks for Scalable, Real Time, Interactive and Digital Media Supercomputing Servers," IBM Journal of R&D Special Issue on Cell Broadband Technology and Systems, Sept. 2007.
- Y. Liu, H. Jones, S. Vaidya, M. Perrone, B. Tydlitat and A.K. Nanda, "Speech Recognition Systems on the Cell Broadband Engine Processor", IBM Journal of R&D Special Issue on Cell Broadband Technology and Systems, Sept. 2007.
- B. D'Amora, A. K. Nanda, K. Magerlein, A. Binstock and B. Yee, "Physics Based On-Line Games on Cell Blades," IBM Systems Journal, Jan 2006.
- K. Keeton, R. M. Clapp and A.K. Nanda, Guest Editors' Introduction: Evaluating Servers with Commercial Workloads, *IEEE Computer,* Feb. 2003, pp 29-32.
- M. Dubois, J. Jeong and A. K. Nanda, "Shared Cache Architectures for Decision Support Systems," *Performance Evaluation,* Vol. 49, Sept. 2002, pp 283-298.
- Y. Hu, Q. Yang and A.K. Nanda, "Measurement, Analysis and Performance Improvement of Apache Web Server," *International Journal of Computers and their Applications*, Dec. 2001
- A. K. Nanda, A-T. Nguyen, M. Michael, D. Joseph, "High Throughput Coherence Control and Hardware Messaging in Everest," *IBM Journal of Research and Development,* March 2001.
- M. Michael, A.K. Nanda and B.H. Lim, "Coherence Controller Architectures for Scalable Shared Memory Multiprocessors", *IEEE Transactions on Computers,* pp. 245-255, Feb. '99.
- A.K. Nanda, J. Bondi and S. Dutta, "The Misprediction Recovery Cache," *International Journal of Parallel Programming*, April 1998.
- U. Ko, P. Balsara and A.K. Nanda, "Power and Performance Optimization for On-Chip Multi Level Cache Hierarchies in Microprocessors", *IEEE Transactions on VLSI Systems*, pp. 299-308, June 1998.

- L.N. Bhuyan, R. Iyer, T. Askar, A.K. Nanda and M. Kumar, "Performance of Multistage Bus Networks for a Distributed Shared Memory Multiprocessor," *IEEE Transactions on Parallel and Distributed Systems,* Jan. 1997.
- A.K. Nanda and L.N. Bhuyan, "Efficient Mapping of Applications onto Cache Coherent Multiprocessors," *Journal of Parallel and Distributed Computing,* Nov. 1993.
- A.K. Nanda and L.N. Bhuyan, "Design and Analysis of Cache Coherent Multistage Interconnection Networks," *IEEE Transactions on Computers,* April 1993.

Refereed International Conferences

- A.K. Nanda, “The Eka Supercomputer”, Keynote paper at HiPC, Dec. 2007, Goa, India.
- A. K. Nanda, K. K. Mak, K. Sugavanam, R. Sahoo, V. Soundararajan, T. B. Smith, "MemorIES: A Programmable, Real-Time Hardware Emulation Tool for Multiprocessor Server Design," ASPLOS 2000, pp 37-48.
- A.K. Nanda, A-T. Nguyen, M. Michael and D. Joseph "High Throughput Coherence Controllers", Proceedings of the 6th International Symposium on High Performance Computer Architecture, HPCA-6, Jan. 2000.
- R. Iyer, L.N. Bhuyan and A.K. Nanda, "Using Switch Directories to Speed Up Cache-to-Cache Transfers in CC-NUMA Multiprocessors", Proceedings of the 12th International Parallel and Distributed Processing Symposium (IPDPS2000), Cancun, Mexico, May 2000.
- M. Michael and A.K. Nanda, "Design and Performance of Directory Caches for Scalable Shared Memory Multiprocessors", Proceedings of the 5th International Symposium on High Performance Computer Architecture, HPCA-5, Jan. 1999.
- Y. Hu, Q. Yang and A.K. Nanda, "Measurement, Analysis and Performance Improvement of Apache Web Server," Proceedings of the 18th IPCCC, Feb. 1999.
- A.K. Nanda, Y. Hu, M. Ohara, M. Giampapa, C. Benveniste and M. Michael, "The Design of COMPASS : An Execution Driven Simulator for Commercial Applications Running on Shared Memory Multiprocessors," Proceedings of International Parallel Processing Symposium, April 1998.
- A.K. Nanda, “Multiprocessor Simulation Techniques”, Keynote Talk at ADCOMP, Dec, 1997, Madras, India
- M. Michael, A.K. Nanda, B-H. Lim and M. Scott, "Coherence Controller Architectures for SMP-Based CC-NUMA Multiprocessors," Proceedings of the 24th International Symposium on Computer Architecture, June 1997.
- A-T. Nguyen, M. Michael, A.K. Nanda, K. Ekanadham and P. Bose `Accuracy and Speed-Up of Parallel Trace-driven Architectural Simulation," Proceedings of International Parallel Processing Symposium, April 1997. .
- A.K. Nanda, J. Bondi and S. Dutta, "Integrating a Misprediction Recovery Cache(MRC) into a Superscalar Processor," Proc. of International Symposium on Microarchitecture, Micro'29, Dec. 1996.
- L.N. Bhuyan, A.K. Nanda and T. Askar, "Performance and Reliability of the Multistage Bus Network," Proceedings of the International Conference on Parallel Processing, August 1994.
- A.K. Nanda and L.N. Bhuyan, "Mapping Applications onto a Cache Coherent Multiprocessor," Supercomputing'92, Nov. 1992.
- A.K. Nanda and L.N. Bhuyan, "A Formal Specification and Verification Technique for Cache Coherence Protocols," Proceedings of the International Conference on Parallel Processing, August 1992.

- A.K. Nanda, D. DeGroot and D. Stenger, "Scheduling Directed Task Graphs on Multiprocessors using Simulated Annealing Algorithms," Proceedings of the 12th International Conference on Distributed Computing Systems, June 1992.
- A.K. Nanda and Hong Jiang, "Analysis of Directory Based Cache Coherence Schemes with Multistage Networks," ACM Computer Science Conference, march 1992.
- L.N. Bhuyan and A.K. Nanda, "Multistage Bus Network(MBN) : An Interconnection Network for Cache Coherent Multiprocessors," Proceedings of the 3rd International Symposium on Parallel and Distributed Processing, Dec. 1991.

PROFESSIONAL INTERVIEWS and SIGNIFICANT NEWS ARTICLES

- Establishment of AHRC at IIT Bhubaneswar, National media coverage, Dec 2023
- Video Interview with Ann Phey on Artificial Intelligence and HPC, IBM Thought Leadership Series, IBM Singapore, Oct 2017.
- Interview with Nicole Hemsoth, HPCWire, “HPC Innovator’s Work Spans Two Continents”, Hamburg, Germany, May 2010
- Interview for IEEE Magazine, Perspectives on New Technologies, Four IEEE Fellows from four Continents, USA, March 2010.
- A.K. Nanda, “The next Challenge in High Performance Computing: Applications and Application Enablement”, Invited Article, HPCWire Online Magazine, Mar 2008
- Chidanand Rajghatta, Senior Editor ToI, “India Hosts World’s Fourth Fastest Supercomputer”, Times of India Front Page Headline Story, New Delhi/New York, Nov 13, 2007
- Interview with Patrick Thibodeau, “India’s Powerful Supercomputer Signals HPC Ambitions”, Senior Editor, Computerworld, Nov 12, 2007, Reno, Nevada, USA

AWARDS/RECOGNITIONS/PROFESSIONAL ACTIVITIES

Fellow: IEEE Computer Society, USA, for Leadership in High Performance Computer Systems

Fellow: Asia Pacific AI Association (AAIA)

Distinguished Alumnus: Sambalpur University (UCE, Burla), Diamond Jubilee, 2017

World’s first PetaFLOP Supercomputer: and world’s fastest supercomputer (LANL Roadrunner machine built at IBM, USA) , Supercomputing - 2008 Conference, Portland, USA, 2008.

Asia’s fastest and World’s 4th fastest Supercomputer: Eka supercomputer (at Tata CRL, Pune, India), Supercomputing - 2007 Conference, Reno, Nevada, USA, 2007.

IBM Awards: Outstanding Technical Achievement Awards, Outstanding Patent Awards between 2000-2007, IBM TJ Watson research Center, NY, USA.

Best Paper/Patent Award: Misprediction Recovery Cache, IEEE Micro Conf, USA, 1995

Fellow selection Committee: member of IEEE Fellow selection committee, USA, multiple times

NSF (National Science Foundation/USA) Research Projects Selection Committee: member, several Times, to select research projects of national/global importance from major US universities and industrial research labs

Journal Editorial Boards: Editorial Board Member of *IEEE Transactions on Parallel and Distributed Systems* Jan. 2001- Dec. 2004. Guest Editor, *IEEE Computer* Special Issue on Work

Loads, Feb. 2003. Guest Editor of Special Issue of IBM Journal of Research and Development (IBM JR&D) on Cell Technology and Systems, Sept. 2007.

Conferences/Invited Talks: General Co-chair of HPCA-7, 7th International Symposium on High Performance Computer Architecture, Monterrey, Mexico, Jan. 2001, Industrial Chair HPCA-16, Keynote talk at International HiPC 2007, Goa, India, Keynote Address at International CAS Conference (USA/Canada), Shanghai, 2004, Keynote Talk at ICPC (USA), 2003, Chennai, India. Steering Committee Member of HiPC 2008/09, Bangalore. Invited talks at MIT, Stanford, UC Berkeley, USC, UIUC, UPenn, UPC Barcelona, IISc, IIT Delhi, IIT Kharagpur, IIT Dhanbad, IIT Mandi, IIT Guwahati, AIIMS Bhubaneswar, IITM Pune, and others.

PhD/MS Thesis Advising: Was co-guide of several MS/PhD students from MIT, Univ of Illinois, Univ of Southern California, and Univ of Rochester. They spent 3-24 months in my labs at IBM TJ Watson Research Center in NY to carry out significant portions of their thesis work. Currently co-guiding 3 PhD, one MS students, and earlier 10 MTech, 25 BTech students at IIT BBSR.

Workshops: Co-founded the first workshop on Computer Architecture Evaluation using Commercial Workloads (CAECW) at HPCA'98 and co-chaired for six years. Co-chaired the Shared Memory workshop at ISCA for three years. Founded and chaired a new workshop on Real Time, Interactive and Digital Media Supercomputing (RIDMS) at HPCA in Feb. 2006.

Program Committee Member: ICCD1995 and 1996, HPCA 1999, 2001, 2005. SIGMETRICS 2001, ISCA 2001, IPDPS, ICDCS and others, ASPLOS 2015.

Referee: IEEE Transactions on Computers, IEEE Transactions on Parallel and Distributed Computing, IEEE computer, Journal of Parallel and Distributed Computing, Parallel Computing Journal, ICPP, ICDCS, ISCA, Supercomputing, Micro, ICCD and HPCA.